TELEDYNE LECROY
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quantumdata™ M42de Display Port 2.1 Video Analyzer/Generator

Key Features

- Equipped with USB-C ports and new enhanced full-size DisplayPort (DP80) connectors for Tx and Rx functions
- Fully supports UHBR sink and source testing at 10Gb/s, 13.5Gb/s and 20Gb/s lane rates with 128b/132b line coding
- Supports DP 1.4 (HBR3) source and sink testing including broad coverage for VESA compliance testing
- View incoming video and metadata (including DSC compressed) from a source device
- Capture and decode video, protocol, control packets including Display Stream Compression (DSC) and Multi-Stream Transport (MST)
- Custom video generator can test displays at HBR and UHBR lane rates with large format and image library
- Configure link training parameters to test display's handling of link training
- Generate Display Stream Compression (DSC), select patterns and configure slices and video parameters
- View and edit EDID and DPCD registers
- Monitor AUX Channel transactions while emulating a DP 1.4 or DP 2.1 source or sink
- Exclusive: T.A.P.4 passive monitoring mode provides visibility to Main Link and AUX Channel traffic for debug of interoperability issues between real DP 2.1 devices
- Test source and sink devices with Panel Replay capability
- Python-based automation API allows running compliance and custom verification tasks in unattended mode
- Support for LTTPR in non-transparent mode for 128b/132b at UHBR rates and 8b/10b encoding for lane rates up to HBR3
- View Power Delivery (PD) protocol negotiations for USB-C DP Alt Mode in the Aux Channel Analyzer utility

The Teledyne LeCroy quantumdata M42de Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol layers for DisplayPort 2.1. The M42de supports legacy DisplayPort HBR3 lane rates of 1.62, 2.7, 5.4, 8.1Gb/s and the new DP 2.1 UHBR lane rates of 10.0, 13.5 & 20.0Gb/s. Now enhanced to support DP80 connections over both USB Type-C® and full size DisplayPort cables, the M42de is your 'one-stop' solution for DP 2.1 testing and certification.

The quantumdata M42de is a highly configurable platform for testing DP 2.1 (and 1.4) source and sink devices with quick real-time views as well as full capture of main line video including meta data and AUX transactions. Invaluable for testing silicon development boards, displays, docking stations, hubs, USB-C adapters, retimers and extenders. The video generator offers a large library of standard video timings and test patterns necessary for easy verification of next generation displays.

The Passive Probe feature based on Teledyne LeCroy's cutting-edge T.A.P.4™ technology, enables full monitoring of the DisplayPort Main Link and the AUX Channel between two DisplayPort devices at the full 20 Gb/s lane rates.

Test Platform Overview

The M42de supports generation and analysis of the DisplayPort data streams through the user-friendly Video Protocol Suite Manager. The M42de features an embedded CPU (linux-based) that operates as a stand-alone platform by connecting an HDMI monitor plus keyboard/mouse (below). Optionally an external laptop can be connected directly to the unit (via RJ45 LAN port) and control the analyzer as a remote PC. Both approaches provide fast access to captured video logs up to 8GB in size.

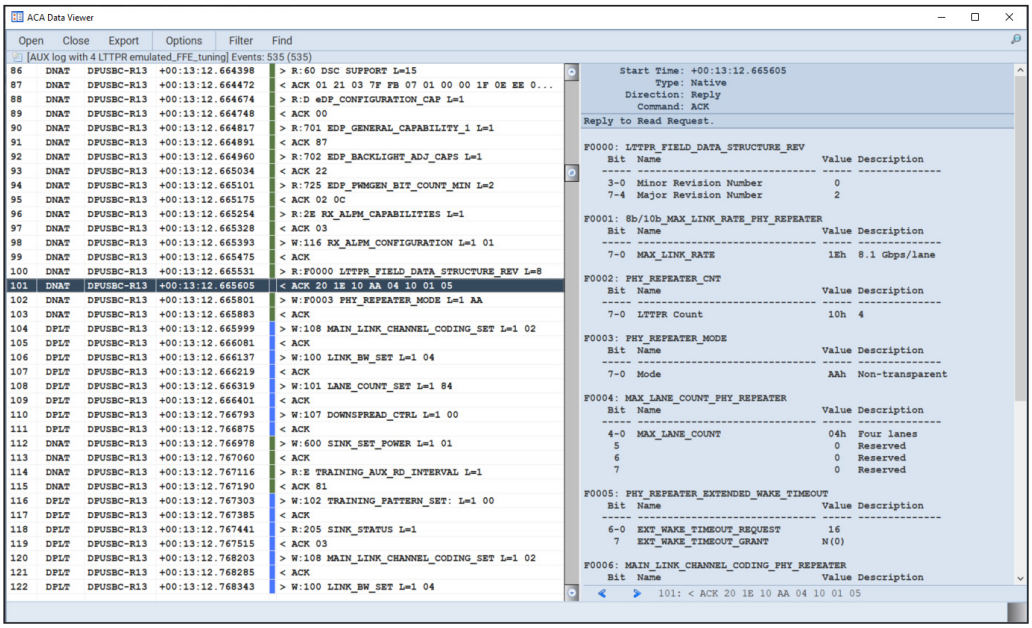
Video Generation

The M42de supports video and audio functional testing at HBR3 / UHBR lane rates on 1, 2 or 4 lanes to support high resolution formats. Users can specify lane configurations for link training and choose from an extensive library of video formats and test patterns.

Display (Sink) Test Setup

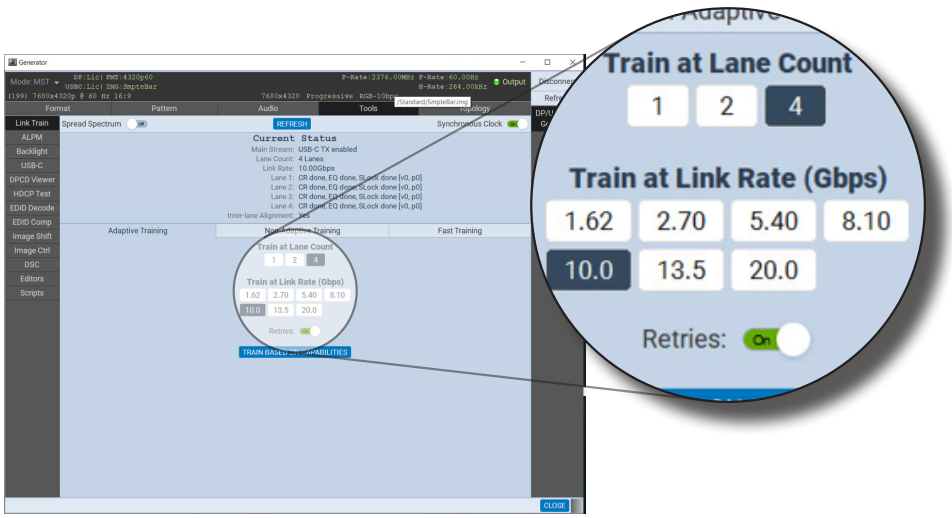
Aux Channel Analyzer (ACA)

The M42de 's Auxiliary Channel Analyzer (ACA) records DP AUX reads and writes to provide insights on link training, MST negotiations, HDCP, DPCD transactions, DP Alt Mode / PD negotiations and EDID exchanges. The ACA captures and timestamps these events allowing users to view each transaction fully decoded. ACA logs can be saved and distributed for off-line analysis by other team members.



Link Training Control and Configuration

The M42de's link training feature provides complete control of link training parameters including lane count and link rate. Convenient controls allow M42de to perform link training dynamically based on the attached device's capabilities; or forcing a specific lane count, link rate, voltage swing, and pre-emphasis.



Generate video source traffic with specific lane count, link rate and resolution with a few clicks.

The M42de fully supports Cable-ID for DP40 / DP80 cables. Operating as a DP sink, it can detect which cable is attached and populate the required DPCD registers. When operating as a DP Alt-mode source, the M42de will automatically read any E-Marked USB Type-C cables attached to the Tx port and configure the link appropriately.

Sink Tests - Control Test Pattern Panel

The M42d 's Video Generator Control Test Pattern panel is the primary interface for customizing generator test functions such as Link Training, Panel Replay, Adaptive Sync, Split SDPs and Link Quality Patterns.

Split SDPs

Control Test Pattern panel enables users to configure the splitting of Secondary Data Packets (SDPs). This panel includes specifying a line number for the SDP location, and optionally configuring the SDP location link clock cycles from the blanking start. The location can also be set automatically (below).

Adaptive Sync

Control Test Pattern Panel allows configuring the Adaptive Sync test patterns (ZigZag or Square Wave). Users have control of the pattern for the ramping up and down of the Adaptive Sync Refresh Rate and the time (in milliseconds) for each incremental increase or decrease in the Refresh Rate (below).

Panel Replay

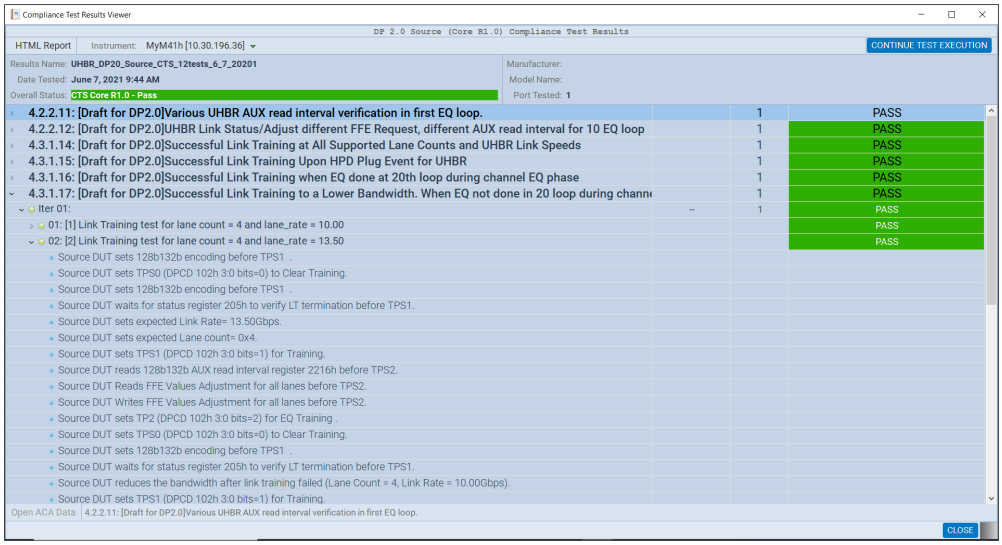
Control Test Pattern Panel enables users to configure the Panel Replay selected updates (SUs) by specifying the interval in number of frames for each SU event. Optionally specify a full frame update to the Remote Frame Buffer also using a specific number of frames.

HDCP Testing

The M42de is fully approved for testing sources, sinks and branch devices for HDCP 2.2/3 compliance.

Broad Coverage of VESA Compliance Tests

The quantumdata M42de provides unmatched support for VESA compliance testing allowing developers to verify functionality, error recovery, and conformance for DisplayPort 1.4 and 2.1 sources, sinks and devices. Seamlessly integrated in the quantumdata analyzer software, the M42de connects directly to the unit-under-test (UUT) over DP40, DP80 or Type-C cables. The M42de mimics real DP source or sink behaviors while capturing the exchange and generating pass/fail reports to provide a fully turnkey test environment. A comprehensive Python-based automation API can run the entire compliance suite or custom test behaviors allowing product teams to boost their utilization and efficiency during the validation cycle.



M42de compliance option automatically logs each test step and generates pass/fail reports

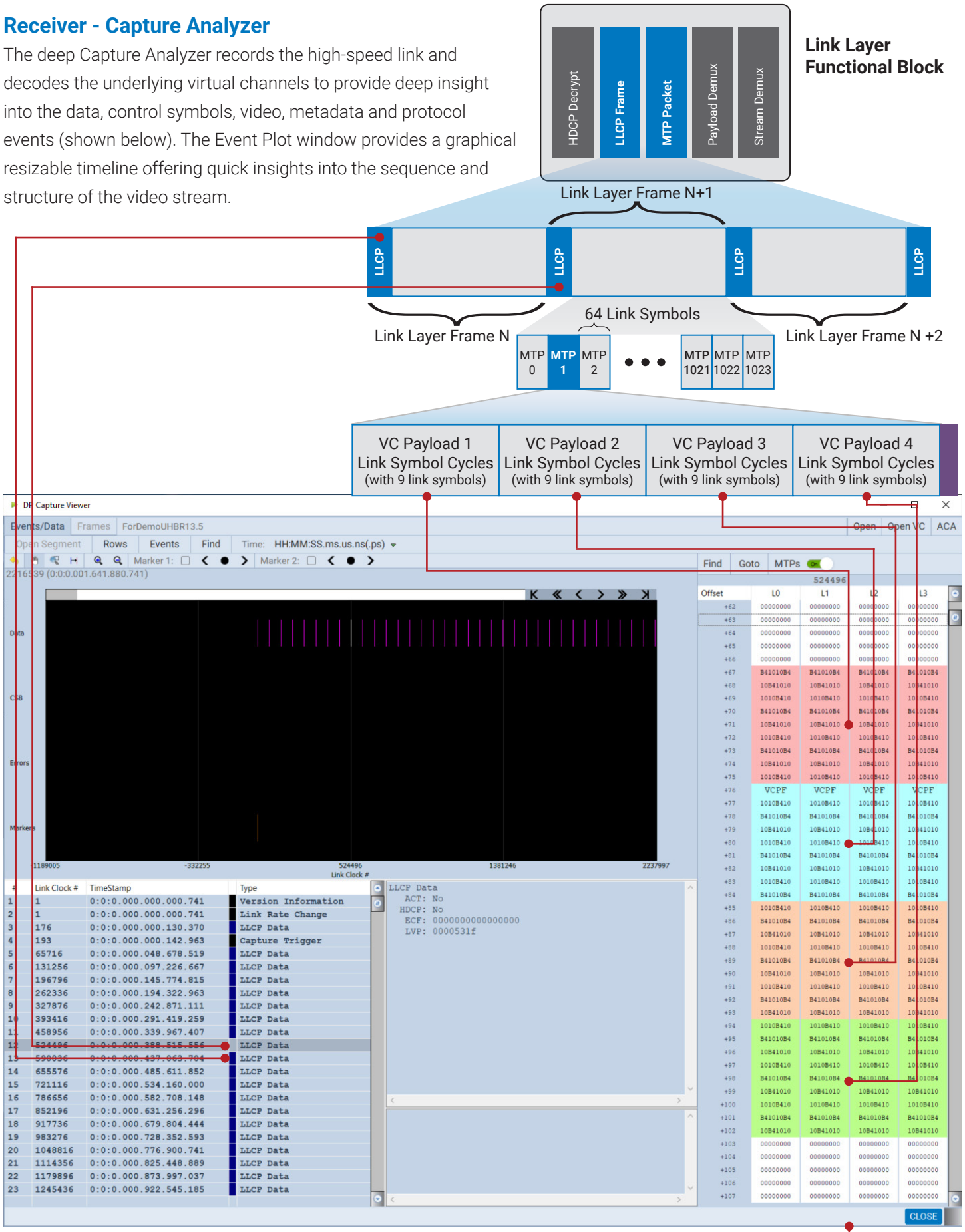
The M42de is recognized by VESA as an approved test solution for DP 1.4 Link Layer, forward error correction (FEC) and display stream compression (DSC) tests. The M42de also leads the industry with an expanding set of DisplayPort 2.1 Link Layer tests (full DP 2.1 test approval is ongoing). The M42de compliance options provide vast coverage allowing DisplayPort chip and device OEMs to save money by performing self-certification in their own lab. The quantumdata team is committed to providing complete coverage of the DP 2.1 link and protocol Compliance Test Suite (CTS) with the regular release of software updates supporting new and updated tests.

Receiver - Basic & Capture Analyzer

The M42de 's Basic Analyzer allows users to view the incoming video, lanes and link rate, timing, colorimetry and various other metadata in real time at a glance. It provides instant confirmation of the negotiated resolution and a representation of the video image. The Rx port emulates any EDID to verify a source can discover and configure a wide range of displays. Similar controls are available in the DPCD Editor to allow emulation of various DP Rx parameters.

Receiver - Capture Analyzer

The deep Capture Analyzer records the high-speed link and decodes the underlying virtual channels to provide deep insight into the data, control symbols, video, metadata and protocol events (shown below). The Event Plot window provides a graphical resizable timeline offering quick insights into the sequence and structure of the video stream.



Complete visibility into Multi-Stream Transport virtual channels including meta data, control and the logical video streams

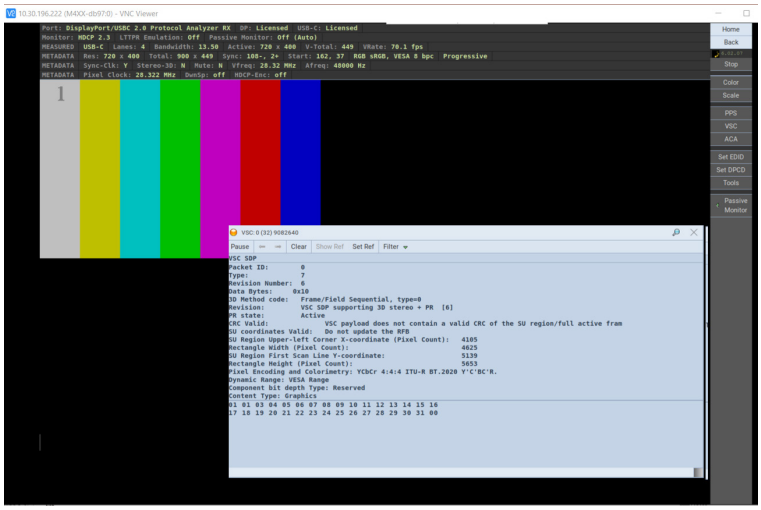
View the underlying virtual channels with a single click

Panel Replay Testing

The M42de supports functional testing of Panel Replay-capable source and sink devices. The capture analyzer can test source behavior by emulating a Panel Replay sink and similar functional test mode for testing Panel Replay capable displays.

Source Analysis

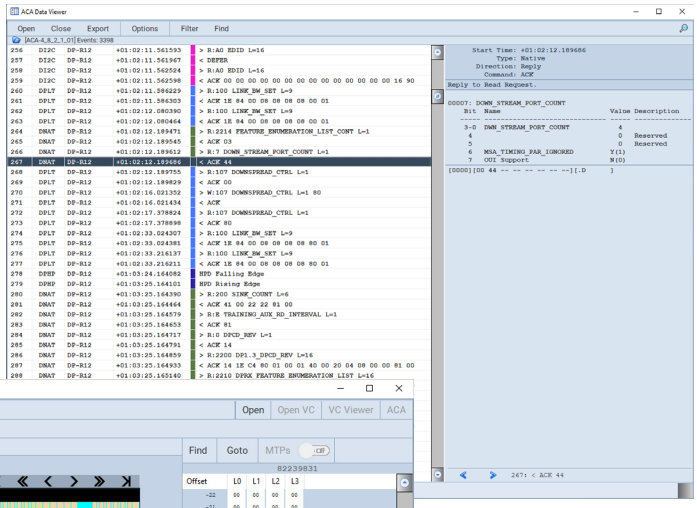
The Real Time analyzer provides a quick view of the incoming Panel Replay VSCs making it easy to see changes from the previous frame. The transaction list shows the Panel Replay VSC metadata packets that have been sent with Selected Update regions. All the critical AUX transactions for discovery and configuration of Panel Replay are also logged.



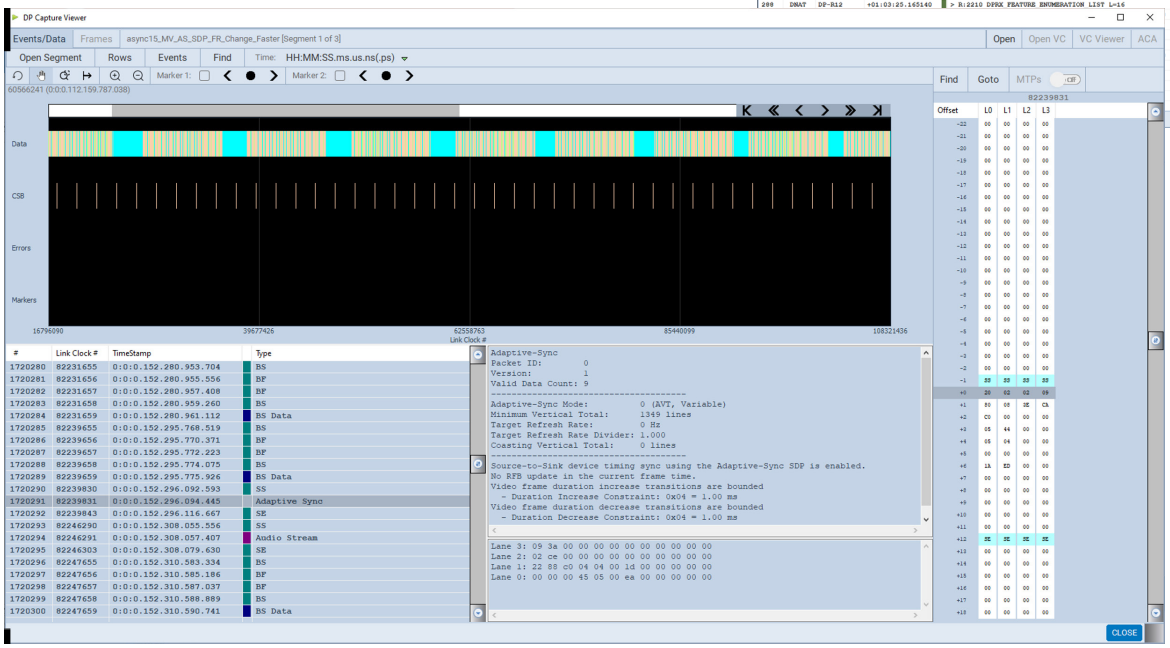
Step through incoming Panel Replay VSCs to view Selected Update regions

Adaptive Sync Functional Testing

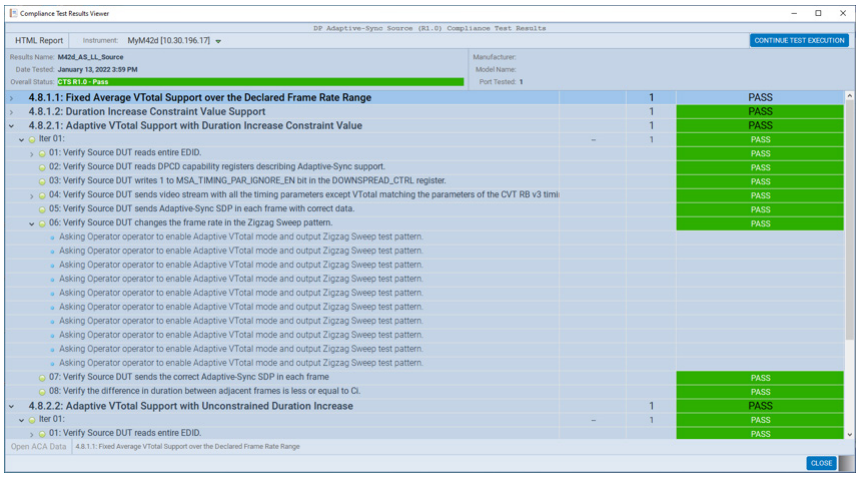
The M42de now supports testing of Adaptive Sync-capable source and sink devices for HBR3 with UHBR in active development. The Adaptive Sync analyzer for source testing enables viewing variations in the vertical blanking to lower the refresh rate. The Adaptive Sync video generator for testing displays enables sending different test patterns that increase or decrease the vertical blanking to verify the refresh rate of the display.



View Adaptive Sync discovery and configuration transactions occurring over AUX with the Aux Channel Analyzer



View the Adaptive Sync variations in the vertical blanking using the Capture Analyzer



Adaptive Sync Compliance Testing

The M42de supports Adaptive Sync compliance testing for both source and sink devices. Sample output provides clear summary of the test result with easy drill-down on each assertion. Fully supports HBR3 with UHBR support in active development. Adaptive Sync compliance test (left) verifies the source can operate in Adaptive VTotal mode (unconstrained) with correct CVT timing parameters.

Source Link Layer Compliance

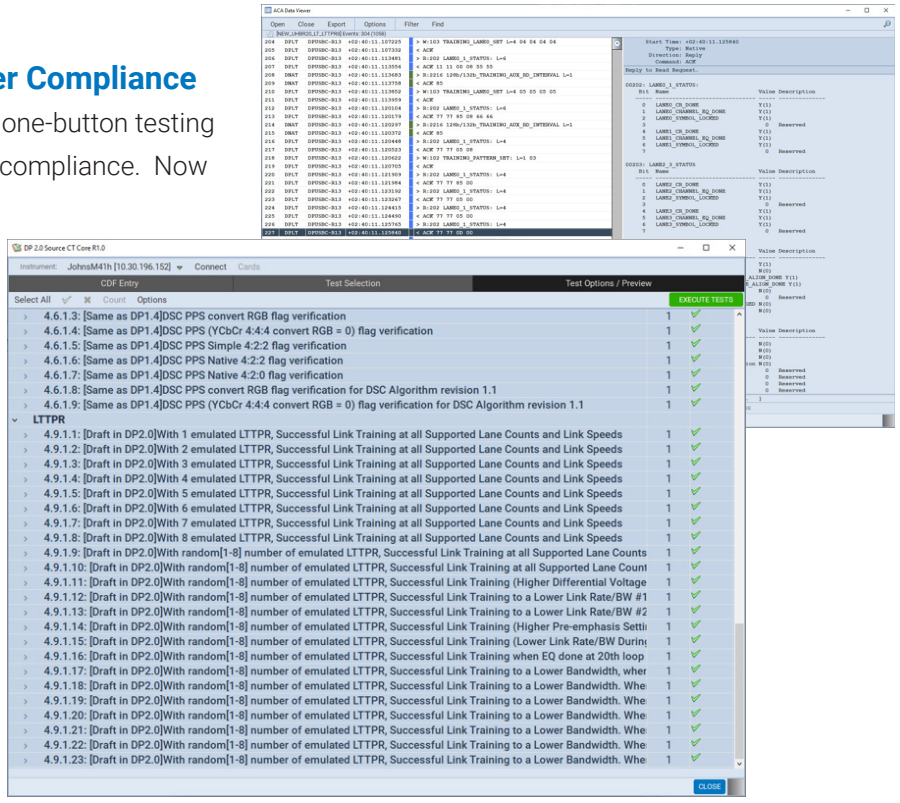
The DP source link layer compliance option is ideal for pre-testing HBR3 or UHBR-capable devices prior to submission to an Authorized Test Center. Pre-testing is considered a critical step in assuring a smooth certification process. The optional compliance test packages allow users to view detailed results and help pinpoint the cause of any failures. AUX channel traces are also saved during Link Layer testing to provide a reliable record of AUX transactions.

Sink Link Layer & EDID Compliance

The DP sink EDID/DisplayID and Link Layer compliance option fully supports DP 1.4 certification and a growing list of DP 2.1 tests. Covering dozens of test cases and hundreds of assertions, the link layer CTS package is foundational for any engineering verification test effort. With essential tests for critical functions including training, forward error correction (FEC), power management and multi-byte AUX transactions, this base package is the starting point for comprehensive test coverage.

LTTPR-Capable Source, Sink & Retimer Compliance

The quantumdata M42de provides automated, one-button testing of Link Training Tunable Phy Repeater (LTTPR) compliance. Now with specific tests for HBR3 and UHBR-capable DisplayPort source, sink and retimer devices, the M42de mimics real LTTPR network behaviors to verify that sources can properly configure and link train in both transparent and non-transparent modes. Simple pass/fail reports are automatically generated and detailed AUX logs are captured which are invaluable for understanding issues during clock data switch phase, equalization, or inter-lane alignment.



Simple pass/fail reports are automatically generated and detailed AUX logs allow quick insight into compliance issues

Specifications

DisplayPort 2.1 Capabilities	
Version	DisplayPort 2.1 (and DP 1.4)
Standard Video Formats	VESA, CTA
Protocols and Line Coding	DP, DSC, FEC, MST, SSC, SDP with 8b/10b and 128b/132b encoding (LTTPR, Panel Replay)
Video Data Rates	1.62, 2.7, 5.4, 8.1, 10.0, 13.5 & 20 Gb/s; 1, 2, 4 Lanes
Video Encoding/Color Depths	RGB, YCbCr - 8, 10, 12, 16 bits
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 1.3 and 2.3
Audio	8 Channel LPCM programmable sine wave
Capture Memory	8 GBytes

Connectors - Front	
DP Standard	Tx (1) Enhanced DP80 full-size; Rx (1) Enhanced DP80 full-size
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for software interface control and external storage media

Connectors - Back	
HDMI Standard	Admin port for connecting external HDMI UHD
USB/USB-C (2 ea.)	Type-C and Type-A for mouse and keyboard
RJ45	Ethernet for connecting to network or host PC running ATP
RCA	SPDIF IN - OUT

Physical/Electric/Admin	
Power	100-240 VAC, 50-60 Hz, 200 Watts
Size / Weight	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm) - 7.6 LBS; 5.057 Kg
Rack mountable	2 RU mounts in 19-inch rack with rack mounting brackets
Internal speaker	Speaker with volume control for monitoring incoming LPCM audio
Command Line Control	Ethernet (RJ-45) for external GUI
System Control	External PC connected over LAN to Ethernet RJ45, VNC or Keyboard/mouse and 4K TV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering Information

Product Description	Product Code
M42de UHBR Video Analyzer/Generator (Hardware system with basic generation and analysis for HBR3 and UHBR rates)	00-00263
M42de HBR3 Video Analyzer/Generator (Hardware system with basic generation and analysis for HBR3 rates)	00-00264
M42de / M42d Upgrade from HBR3 systems (00-00261 or 00-00264) to enable UHBR rates	95-00221
Passive Probing Main Link and AUX Channel	95-00222
Sink Enhanced Functional test - Includes DSC, LTTPR, Panel Replay & Adaptive Sync Functional Tests	95-00225
Source Enhanced Functional test – Includes DSC, Capture Analysis, LTTPR, Panel Replay, Adaptive Sync Functional	95-00226
DP 1.4 Sink EDID/DisplayID compliance tests (requires 95-00225)	95-00227
DP 1.4 Source EDID/DisplayID compliance tests (requires 95-00226)	95-00228
DP 1.4/2.1 Source Link Layer & (MST future) compliance tests (requires 95-00226)	95-00232
DP 1.4/2.1 Sink Link Layer & (MST future) compliance tests (Limited DP 2.1 tests currently supported; full suite future) (requires 95-00225)	95-00233
DP 1.4/2.1 DSC/FEC Source compliance tests (DP 2.1 tests are future) (requires 95-00226)	95-00236
DP 1.4/2.1 DSC/FEC Sink compliance tests (DP 2.1 tests are future) (requires 95-00225)	95-00237
DP 1.4/2.1 LTTPR Source compliance tests (requires 95-00226)	95-00240
DP 1.4/2.1 LTTPR Sink compliance tests (requires 95-00225)	95-00241
DP 1.4/2.1 LTTPR Device compliance tests (requires 95-00225 & 95-00226)	95-00242
DP 1.4/2.1 Adaptive Sync Source compliance test (support for DP 2.1 UHBR rates is future) (requires 95-00226)	95-00234
DP 1.4/2.1 Adaptive Sync Sink compliance test (support for DP 2.1 UHBR rates is future) (requires 95-00225)	95-00235
HDCP 2.3 Source compliance tests (requires 95-00226)	95-00214
HDCP 2.3 Sink compliance tests (requires 95-00225)	95-00217
Embedded DisplayPort (eDP) (Limited functions supported)	95-00212
M41x Rack-mount Kit	95-00209

Local sales offices are located throughout the world.
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